APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

RAKE RECEIVER INTERFACE

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RAKE RECEIVER INTERFACE

BACKGROUND OF THE INVENTION

[0001] A code division multiple access (CDMA) receiver may comprise a rake receiver, which may include multiple receiving elements, called fingers, which de-spread a received signal. A finger may be synchronized to a path of a multi-path channel between a base station and a mobile receiver. Information, such as symbols bounded by symbol boundaries, may be transferred from the fingers to a processor.

[0002] However, the timing of one finger may change independently of another finger, due to such factors as a dynamic environment and movement of the mobile station, for example. The lack of synchronization of the fingers may make it difficult for the processor to recognize the symbol boundaries for a particular finger.

[0003] In one possible solution, a finger may generate "interrupts" at a rate synchronized to the symbol boundary rate of the finger. The processor may read and process a fixed number of symbols between successive interrupts. For example, if the interrupt rate were equal to the symbol rate, then the number of symbols bounded by successive interrupts would be equal to the number of symbols bounded by successive symbol boundaries.

[0004] A disadvantage of the abovementioned interrupt method may be that a very large processing and memory overhead may be required to process a large number of fingers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

[0006] Fig. 1 is a simplified block diagram of a method and apparatus for interfacing with a rake receiver, in accordance with an embodiment of the invention;

[0007] Fig. 2 is a simplified block diagram of fingers of a rake receiver, having symbol boundaries with different rates, and with interrupts generated at a rate independent of the symbol boundary rates, in accordance with an embodiment of the invention;

[0008] Fig. 3 is a simplified illustration of generating interrupts in the transfer of symbol boundaries to a processor, in accordance with an embodiment of the invention, wherein the timing of the fingers may remain constant;

[0009] Fig. 4 is a simplified illustration of a "collision" between "reading to" and "writing from" the same data register, wherein the timing of the fingers may vary;

[0010] Fig. 5 is a simplified illustration of an embodiment of the invention that may prevent such a collision, wherein the timing of the fingers has advanced; and

[0011] Fig. 6 is a simplified illustration of an embodiment of the invention that may prevent such a collision, wherein the timing of the fingers has retarded.

[0012] It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF THE INVENTION

[0013] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However it will be understood by those of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

[0014] Reference is now made to Fig. 1, which illustrates a method and apparatus for interfacing with a rake receiver, in accordance with an embodiment of the invention.

[0015] The apparatus may comprise one or more fingers 10 of a rake receiver 11, which may transfer information to a processor 12, as seen in Fig. 1. Processor 12 may comprise, without limitation, a digital speech processor (DSP). The information may comprise, without limitation, symbols having symbol boundaries. For example, as seen in Fig. 2, a first finger F1 may comprise symbol boundaries 16A-16D, which may have a certain time rate, e.g., a time spacing between adjacent symbol boundaries. The symbol boundaries may correspond to a spreading sequence epoch, for example. A second finger F2 may comprise symbol boundaries 18A-18D, which may have a different rate.

[0016] Interrupts 19 (Fig. 2) may be generated by hardware or software apparatus (such as but not limited to, the fingers, rake receiver or processor or some dedicated device for generating interrupts, for example) in the transfer of information between the rake receiver 11 and processor 12. In accordance with an embodiment of the present invention, the interrupts may have a rate of generation per unit time independent of a rate of the transfer of information per unit time. In the illustrated embodiment, the interrupts are generated in the transfer of symbols between fingers 10 and processor 12, wherein the interrupts have a rate of generation independent of a time rate of the symbol boundaries (e.g., time spacing between adjacent symbol boundaries). For example, the interrupts may be generated with a rate asynchronous with respect to the time rate of the symbol boundaries 16A-16D or 18A-18D, such as, but not limited to, a fixed time rate.

[0017] The apparatus of Fig. 1 may form part of a communications system, such as but not limited to, a code division multiple access (CDMA) or wide-band CDMA

(WB-CDMA) receiver or communications system, which may comprise communications components.

[0018] Reference is now made to Fig. 3, which illustrates one embodiment of the invention for generating interrupts in the transfer of symbol boundaries to the processor 12. The timing of the interrupts may be defined as global symbol boundaries 20A-20C, which may be generated at a rate independent of the time rate of symbol boundaries 16A-16D and 18A-18D.

[0019] Two fingers F1 and F2 may write data (e.g., symbols from the respective symbol boundaries) to either of first and second data registers R0 and R1. It is noted that this is merely a simplified example, and the invention is not limited to two fingers or data registers, and may employ any other number of fingers or data registers. Fig. 3 illustrates the case wherein the timing of the fingers F1 and F2 may remain constant, and wherein the global symbol boundaries 20A-20C may have a fixed rate. For example, starting at a symbol boundary 16A and ending at a symbol boundary 16B, finger F1 may write information (e.g., symbols) to first data register R0. Afterwards, starting at symbol boundary 16B and ending at a symbol boundary 16C, finger F1 may write information to second data register R1, and so on. Likewise, starting at a symbol boundary 18A and ending at a symbol boundary 18B, finger F2 may write information (e.g., symbols) to second data register R1. Afterwards, starting at symbol boundary 18B and ending at a symbol boundary 18C, finger F2 may write information to first data register R0, and so on.

[0020] The global symbol boundaries 20A-20C may determine how the processor 12 reads the information. The rate (or also referred to as the length) of the global symbol boundaries 20A-20C may be set such that the processor 12 may read alternately from the data registers independently of the rate at which the fingers F1 and F2 write to the data registers. For example, starting at a global symbol boundary 20A and ending at a global symbol boundary 20B, the processor 12 may read information received from finger F1 from first data register R0, and information received from finger F2 from second data register R1. Afterwards, starting at global symbol boundary 20B and ending at a global symbol boundary 20C, the processor 12 may read information received from finger F1 from second data register R1, and information received from finger F2 from first data register R0, and so on.

[0021] Accordingly, in the embodiment of Fig. 3, the first and second fingers F1 and F2 may write to an available one of the first and second data registers, and in the global symbol boundaries, the processor may alternatively read from the first and second data registers at a rate independent of the fingers. The data registers may be toggled by the fingers during "write", and toggled by the processor 12 during "read".

[0022] As mentioned hereinabove, Fig. 3 illustrates the case wherein the timing of the fingers F1 and F2 may remain constant, and wherein the global symbol boundaries may have a fixed rate. The global symbol boundaries may be set such that while the processor 12 may be reading symbols of the first finger F1 from the first data register R0, for example, the first finger F1 may not be writing at that time to data register R0. Likewise, while the processor 12 may be reading symbols of the first finger F1 from the second data register R1, for example, the first finger F1 may not be writing at that time to data register R1. Accordingly, no information may be written over by the fingers in the data registers while reading from the data registers. Moreover, a data register may always be available for a particular finger to write thereto, while the processor 12 is reading from another data register. This may prevent missing information from one of the fingers due to a lack of an available data register.

[0023] Reference is now made to Fig. 4, which illustrates a case wherein the timing of one of the fingers (e.g., the rate of the symbol boundaries) may vary with time, such as may happen during time tracking, for example. Although processing techniques may be used to vary the global symbol boundaries in accordance with the variance in the timing of the fingers, it may be advantageous and cost-effective to maintain the global symbol boundaries at a fixed rate.

[0024] In Fig. 4, the global symbol boundaries 20A-20E have a fixed rate. The rate of the symbol boundaries 16A-16E of finger F1 may change. For example, the rate of the symbol boundaries may advance (in other words, become shorter) while writing to data register R1 as opposed to data register R0. As indicated by reference arrow 25, between symbol boundaries 16D and 16E, this may lead to the situation wherein the finger F1 may write to data register R0 at the same time that the processor may be reading from data register R0. There is thus a "collision" between "reading to" and "writing from" the same data register. A similar problem may occur as a result of "hold" operations, wherein the effective symbol length may be increased.

[0025] Reference is now made to Fig. 5, which illustrates an embodiment of the invention that may prevent such a collision. The apparatus of Fig. 1 may be provided with one or more counters 22. When a finger writes to one of the data registers, the counter 22 may be incremented. Conversely, when the processor 12 reads from one of the data registers, the counter 22 may be decremented. The counter 22 may be incremented or decrement by one or any other predetermined value.

[0026] In the embodiment of Fig. 3, wherein the timing of the fingers F1 and F2 may remain constant, the sequence of the counter values would be +1, 0, +1, 0, +1 ...

[0027] However, in the embodiment of Fig. 5, the rate of the symbol boundaries 16 of finger F1 may change with time. As indicated by reference arrow 27, when the finger F1 writes to data register R0, the counter 22 (Fig. 1) may be incremented +1. At the same time, the processor 12 may read from data register R1, which may decrement the counter 22 to 0, as indicated by reference arrow 29. Afterwards, the finger F1 may write to data register R1, and the counter 22 may be incremented +1, as indicated by reference arrow 31, whereas the processor 12 may read from data register R0, which may decrement the counter 22 to 0, as indicated by reference arrow 33. However, the timing of finger F1 may have advanced, with the result that finger F1 may start writing to register R0 before the processor 12 has completed reading from data register R0, as indicated by reference arrow 35. This may increment the counter 22 by +1 to +2. In accordance with an embodiment of the invention, if the counter 22 reaches +2 or any other predetermined value, an "extra flag" may be raised, instructing the processor 12 to read both registers R0 and R1, to which finger F1 has written, in the same global symbol boundary, as indicated by reference arrow 37, before reading from another global symbol boundary. The act of reading from two registers may double decrement the counter 22 back to zero. After the counter 22 has returned to zero, the normal sequence of toggling (alternatively reading and alternatively writing) between 0 and +1 (such as the sequence associated with the embodiment of Fig. 3) may be restored.

[0028] Reference is now made to Fig. 6, which illustrates an embodiment of the invention that may prevent a read-write collision, wherein the timing of the finger F1 slows down.

[0029] As indicated by reference arrow 40, when the finger F1 may write to data register R0, the counter 22 may be incremented +1. At the same time, the processor 12 may read from data register R1, which may decrement the counter 22 to 0, as indicated by reference arrow 41. Afterwards, the finger F1 may write to data register R1, and the counter 22 may be incremented +1, as indicated by reference arrow 42, whereas the processor 12 may read from data register R0, which may decrement the counter 22 to 0, as indicated by reference arrow 43. Once again, the finger F1 may write to data register R0, and the counter 22 may be incremented +1, as indicated by reference arrow 44, whereas the processor 12 may read from data register R1, which may decrement the counter 22 to 0, as indicated by reference arrow 45.

[0030] However, the timing of finger F1 may have slowed down, with the result that finger F1 may still be writing to register R0 when the processor 12 has completed reading from data register R1 and starts reading from register R0, as indicated by reference arrow 46. This may decrement the counter 22 by -1 from zero to -1. In accordance with an embodiment of the invention, if the counter 22 reaches -1 or any other predetermined value, an "old flag" may be raised, instructing the processor 12 not to switch to read another data register (in this example, not to switch to data register R0), but rather to continue reading from the current data register to which finger F1 has written (in this example, data register R1), as indicated by reference arrow 47, and to zero the counter 22.

[0031] After the counter 22 has returned to zero, the normal sequence of toggling between 0 and +1 (such as the sequence associated with the embodiment of Fig. 3) may be restored.

[0032] While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those of ordinary skill in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.